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SEMI-ANNUAL TECHNICAL REPORT FOR THE COMMON AFFORDABLE RADAR PROCESSOR (CARP)

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1 INTRODUCTION

1.1 Background

The Office of Naval Research (ONR) Surface/Aerospace Surveillance technology program is conducting technology investigations and development of advanced radar signal and control processor technology for current and planned radar systems. The "Common Affordable Radar Processor (CARP)" project is investigating new processor hardware, networks, and software architectures, which can readily accept integration of new radar signal inputs, digital signal processing techniques/algorithms, system control implementations, and software system infrastructures. The project emphasizes application of state of technology Commercial-Off-The-Shelf (COTS) open architecture processing and networking solutions to Navy radar and combat system needs. The contractor will leverage the successful technological advances developed to date for CARP and use these capabilities as a foundation to research, develop, integrate and test the next generation CARP system leading to a migration and technology transition to 6.4 production programs.

1.2 Scope

The scope of this report is to document CARP program activities supporting contract Delivery Order 011 (DO-011) completed in the semi-annual period from May 19, 2005 to November 19, 2005. The report states research and development objectives followed by a detailed description of continuing progress on the following CARP system enhancements and additions:

- Enhancing the Data Distribution Module (DDM) Subsystem, including Column Beamforming
- Increasing system scalability
- Digital Receiver/Exciter (DREX) test scaffolding enhancement
- Digital Signal Processing (DSP) Subsystem development
- DSP hardware evaluation and subsystem sizing and timing
- Communication library automated performance measurement
- Continued optimization of previously delivered applications
- Human Machine Interface (HMI) Subsystem enhancement to support new system functions
- Embedded and Orthogonal control scheme support
- Open System/Subsystem Interface specification

The report identifies the configuration management processes performed during development, and also includes a section on plans for the next semi-annual period.

2 SYSTEM DEFINITION

2.1 Objectives

The overall CARP System objective is to develop an open architecture receive processing system solution which is directly scaleable to future naval surface ship requirements for large phased array radar systems.

2.2 Requirement Definition

Requirements definition for the Build 4 CARP system was undertaken under contract Delivery Order 005 (DO-005) and revisited for DO-011 in this semi-annual period. Goals for the Build 4 system include significantly increased capabilities in the DDM, DSP, RC and HMI Subsystems:

- DDM FPGA based channel processing including digital down conversion Equalization Filtering (upgraded from previous builds)
- Full Digital Beamformation in azimuth and elevation dimensions for large phased array radar systems
- Increased maximum digital DDM input signal bandwidth to 160+ MHz
- DDM Subsystem throughput and bandwidth up to 60 Mega Samples Per Second (MSPS)
- Demonstrable scalability across system processing elements
- Support for multiple control schemes
- Server based Radar Control including Radar Event scheduling
- An Enhanced DSP suite with extended data representation and DSP subsystem control
- An Enhanced HMI Subsystem including system control and status interfaces and data rendering
- DREX test scaffolding design, emphasizing DDM design reuse
- Open Interface Specification

2.2.1 Build 4 Conceptual Design Overview

The CARP system provides a common processing platform for radar systems with built-in support for open system interfaces. By providing a modular, flexible, scalable architecture, the design can be configured to meet the requirements of a multitude of radar systems. The long term focus of the project is to support Intermediate Frequency (IF) signal reception of digital packet data and transmit signal generation/control messages, perform signal transmission/reception, carry out digital beamforming of received signals across multiple channels (along with down conversion and channel to channel equalization), and apply additional “downstream” signal processing on the generated beam data in commercially available computer processors. Built in testability, including loop-back and self test, is also an important goal.

In the CARP approach for Build 4, the system is composed of four integrated subsystems: a DDM Subsystem, a Radar Controller Subsystem, a Digital Signal Processing Subsystem, and an HMI subsystem. The figure below (Figure 1: Build 4 Conceptual Design) shows the conceptual design of the Build 4 System and includes the four subsystems of the current architecture with a notional DREX test scaffolding block (this is actually physically provided by the DDM Subsystem in Build 4) and an external combat system. Subsystem definitions are included in Section 3, Development Activities.

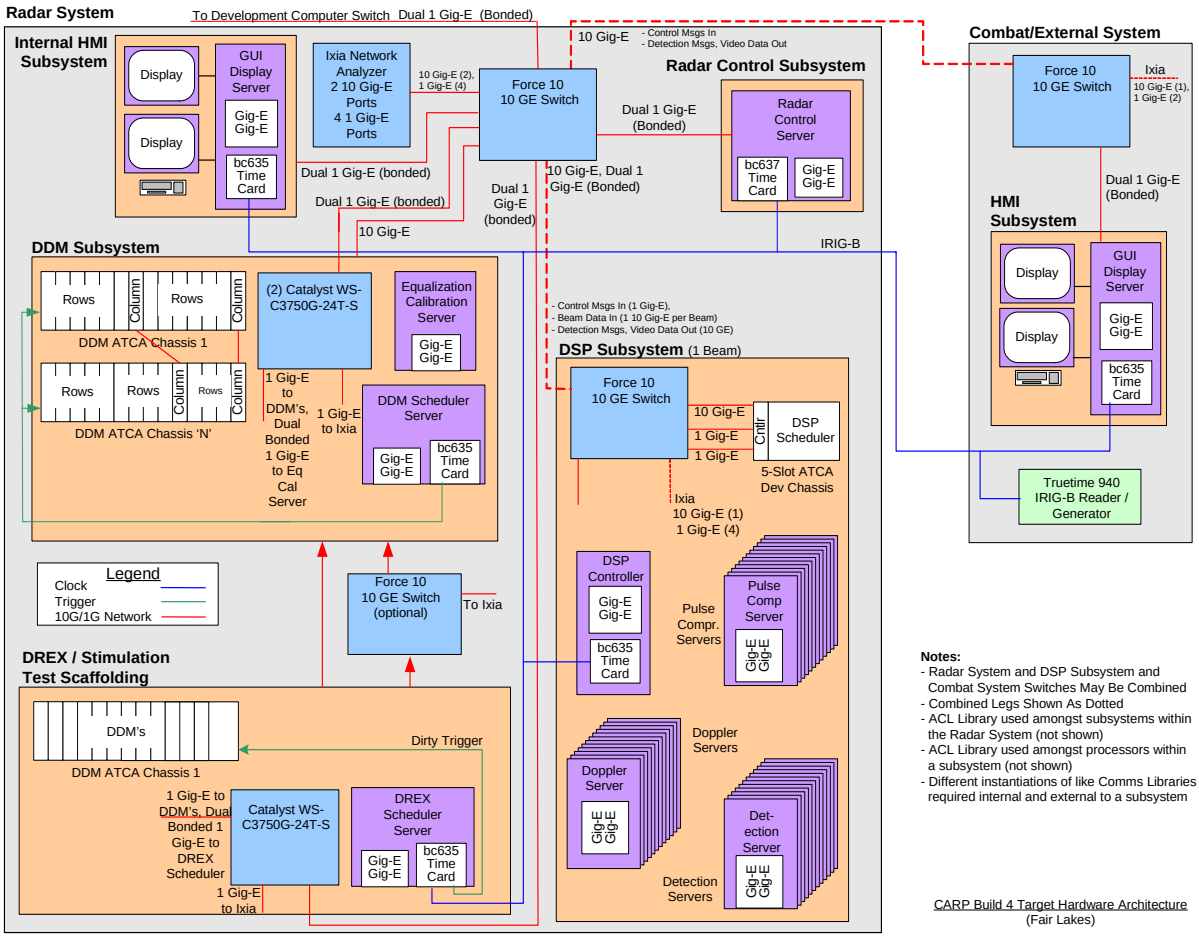

Figure 1: Build 4 Conceptual Design

2.3 Requirements

Requirements for the Build 4 system were defined to meet all targets and included specifications for system interfaces, control schemes, signal performance and integrity through all signal processing stages, testability, and system performance goals.

2.4 Modeling and Analysis

Parallel to system design efforts, most processes of the CARP system are modeled and analyzed to verify algorithms and functionality. Other Government-provided studies were also utilized during this phase of the project.

2.5 Configuration Management

As in previous CARP Builds, Configuration Management was handled by the Concurrent Versions System (CVS), an open source version control suite. Separate repository trees were maintained for CARP Software, Firmware and Matlab models. More information on CVS is available at www.cvshome.org.

3 DEVELOPMENT ACTIVITIES

CARP Activities in the first semi-annual period of the DO-011 contract included continuing development of the DDM, RC, DSP and HMI Subsystems, enhancement/optimization of associated Communication Libraries and Applications delivered under DO-005 and previous CARP Builds, plus progression on an Open Interface Specification for the CARP system.

3.1 DDM Subsystem

The CARP Build 4 DDM (design delivered under DO-005) is a high performance embedded computing board designed to meet future radar needs in digital channel processing and digital beamforming (Figure 2: the CARP Build 4 DDM). It utilizes state-of-the-industry commercial components to harness technology progression and has designed-in flexibility and modularity to enable integration with multiple system implementations. The CARP DDM Subsystem includes DDM Boards along with control and other complimentary applications. The following sections identify DDM Subsystem tasks in progress during the first semi-annual period of the DO-011base task.

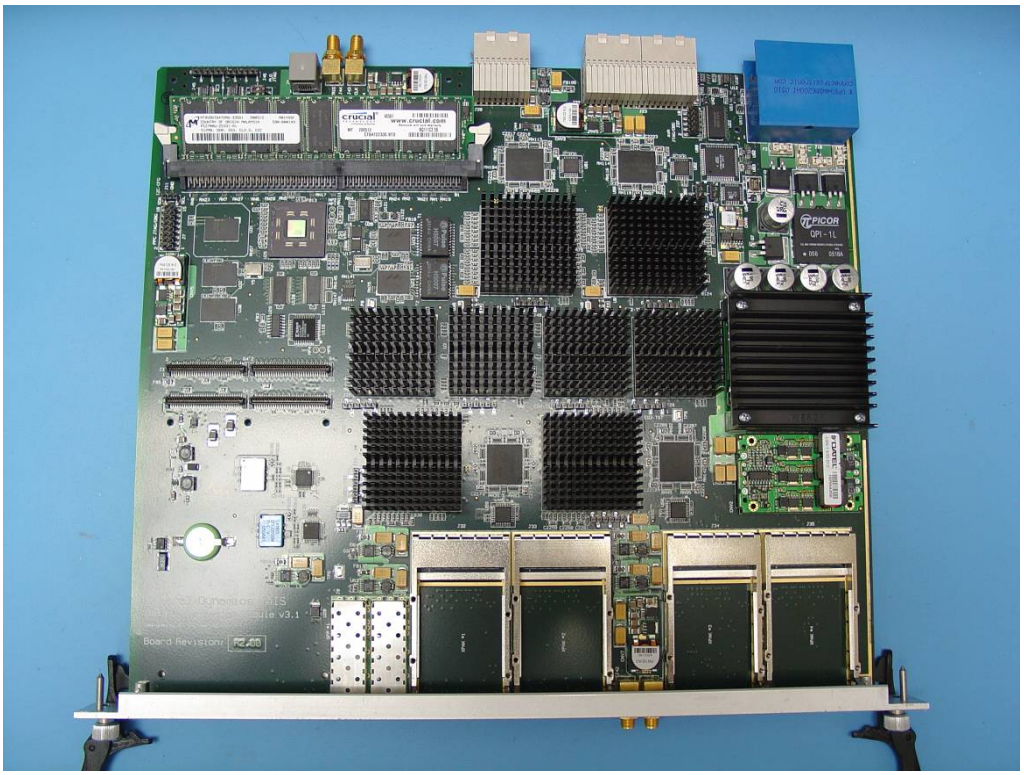

Figure 2: the CARP Build 4 DDM

The CARP DDM Subsystem is designed to perform digital beamforming using a Row-Column approach. Row Beamformer DDMs (delivered in DO-005) receive channel data and form Azimuth-Beams. The functions of the Column Beamformer DDMs (still in development) are to form Elevation-Beams from the Row Beamformer

(azimuth-beam) data, then package their output into Open Interface-compliant messages and transmit it via 10 Gigabit Ethernet based on industry standard Internet Protocol (IP).

3.1.1 Scalability

The Row-Column beamforming approach identified above is enabled through the use of an Advanced Telecom Communications Architecture (ATCA) backplane for intra-DDM board data passing. Multi-board communication in the subsystem target-rack setup has been verified. This approach to digital beamforming makes for a highly scalable architecture where the subsystem input channel configuration can be increased by simply connecting additional DDM boards to the backplane.

The final channel/beam configuration for Build 4 is still under consideration and will be dependant on the number of functional DDM boards produced. It is not limited by the subsystem architecture.

3.1.2 Digital Interface

A bi-directional 10GE digital interface has been implemented for IF data acquisition into the Build 4 DDMs, with each physical interface handling the aggregation of two channels for 16 bit data. The messaging format accepted by the interfaces is Open Interface compliant and follows IEEE standards.

3.1.2.1 Increased Input Sample Rate Support

The DDM Team has verified the subsystem is capable of processing an input signal data rate of 160 MSPS and is currently testing the viability of running at 200 MSPS (DO-011 Base Task goal was 160 MSPS +).

3.1.3 DDM Controller Application Optimization

The DDM Subsystem delivered in DO-005 included a DDM controller application that runs locally on DDM boards and controls their data management and processing. The measured performance of the application and the board functionality it controls was delivered also. Optimization of this application's functionality, especially related to board setup in preparation for received radar events, is in progress in DO-011.

3.1.4 Row Beamformer Digital Signal Processing

DDM Channel Processing (including Digital Down Conversion, Equalization Filtering), and Row Beamforming have been carried from previous builds. Expansion of the dynamic range in each stage of the processing stream is a goal for DO-011 and is under investigation.

3.1.5 Column Beamforming Field Programmable Gate Array (FPGA) Control Code

Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL) control code for installation in the Column Beamformer DDM's Beamformer FPGAs has been generated using Xilinx Integrated Software Environment (ISE) and simulated using Aldec Active-HDL. Its purpose is to handle the beamforming operation and transmit logic.

Work on the Column Beamformer component of the DDM Subsystem is still in progress.

3.1.6 Expansion of DDM Subsystem Output data width to 32 bit Floating Point Samples

VHDL Column Beamformer data output logic to expand DDM Subsystem Beam Data Output to 32 bit floating IEEE Standard point samples (32 bits Inphase, 32 bits Quadrature) was generated and simulated, and will be a significant increase from the 16 bit short sample width delivered in DO-005.

3.1.7 DREX Simulation Test Scaffolding

To provide the Build 4 system with digital data stimulation, "loopback" functionality was built into the DDM Boards of the DO-005 DDM Subsystem to issue locally-stored data files back into DDM input receive logic. For DO-011, development of these functions is continuing with the goal of providing a simulation of the DREX interface to the system.

3.1.8 DDM Subsystem Hardware

The DDM Subsystem Hardware supporting DO-011 Base Task development includes:

- DDM Boards (25) and associated components–
  - Xilinx Virtex-II Pro P40 (4 per board)
  - Xilinx Virtex-II Pro P70 (4 per board)
  - 440GX PowerPC
- Schroff Advanced TCA 12 U Integrated System Chassis
  - P/N# 11592 451
- Apple Xserve
  - Dual 2.3 GHz PowerPC G5 Processors
  - 2 GB SDRAM , 1.35 GHz Frontside Bus
  - Dual On-Board 1GE Gigabit Ethernet
- Symmetricom bc635 timing card for subsystem synchronization
- Cisco Catalyst WS-C37506-24T-S 1 GE Switch (2)

3.2 DSP Subsystem

The CARP Build 4 DSP Subsystem (planned for integration in the next semi-annual period) is comprised of a suite of DSP Applications, a Subsystem Scheduler, a Subsystem Controller and an interface capable of receiving the high bandwidth output of the DDM subsystem. It is designed to utilize high density COTS server technology to provide signal processing including Pulse Compression, Doppler Processing and Detection Processing to the system in a highly scalable architecture. The following sections list DSP Subsystem task progress in this semi-annual period.

3.2.1 DSP Subsystem Scheduling Algorithm Analysis

DSP Subsystem design (in development for DO-011) includes a DSP Scheduler application designed to track availability of running DSP programs to allow scheduling of data processing with the intent of maximizing subsystem throughput and density.

Currently DSP Scheduler's process scheduling algorithm design is underway and is subject to analysis of system models based on measured DSP application performance values.

3.2.2 Hardware Evaluation, Sizing and Timing

DSP Subsystem design is subject to tight form factor and performance goals. Evaluation of high density Linux-based COTS server DSP Subsystem Architecture candidates was completed and delivered in DO-005. The DO-011 effort continued the analysis of the chosen IBM Bladecenter configuration and so far has focused on configuring the purchased Bladecenter and the benchmarking of CARP DSP Applications running on the JS20 Blades.

3.2.2.1 Bladecenter Configuration

The fully populated Bladecenter assembly has been received and assembled; configuration in preparation for integration in the DSP Subsystem is underway (see Figure 3: IBM Bladecenter).

Figure 3: IBM Bladecenter

3.2.2.2 Application Performance Measurement

Measured performance of Build 3 CARP DSP applications was delivered with DO-005 as part of DSP Subsystem Hardware Evaluation tasking. Benchmarking is a continuing effort in DO-011.

The bulk of the current effort is development of testing tools designed to automate performance measurement using the Application Programming Interface of an Ixia Network Traffic Generator/Analyzer.

3.2.3 DSP Application Enhancement

The CARP Build 4 DSP Subsystem includes Pulse Compression, Doppler Processing and Detection Processes carried up from the Build 3 system. Optimization and functional improvement of those applications is in progress in preparation for DSP Subsystem Integration.

3.2.4 Extended Data Width

To increase system processing gain and maximize dynamic range, DSP Subsystem application data processing and message-transfer data widths are being extended from 32 bits to 64. This upgrade is in progress.

3.2.5 DSP Subsystem Hardware Enhancement

DSP Subsystem Hardware supporting DO-011 Base Task development includes:

- eServer Bladecenter Chassis
- Bladecenter JS20 Servers
  - Dual PowerPC 970 2.2 GHz
  - Dual Gigabit Ethernet
- Symmetricom bc635 timing card for subsystem synchronization

3.3 RC Subsystem

The RC Subsystem provides Radar Control to the CARP system (similar to previous builds). Its main functions are System Resource Management and Radar Event Scheduling. A version of the subsystem and RC application was delivered under DO-005. Optimization of the RC Scheduling function is a continuing focus of the DO-011 effort.

3.3.1 Radar Event Scheduling Algorithm Analysis and Development

RC Radar Event scheduling sorts operator issued Radar Event Requests into Radar Event Messages to control system radar operation. The current algorithm in use is being analyzed and updated in Matlab Models in an attempt to increase response time of the system for servicing Radar Event Requests.

3.3.2 RC Subsystem Hardware Enhancement

RC Subsystem Hardware supporting DO-011 Base Task development includes:

- Apple Xserve
  - Dual 2.3 GHz PowerPC G5 Processors
  - 2 GB SDRAM , 1.35 GHz Frontside Bus
  - Dual On-Board 1GE Gigabit Ethernet
- Symmetricom bc635 timing card for subsystem synchronization

3.4 HMI Subsystem

The HMI Subsystem provides the Operator Interface to the CARP System, and is carried over from the DO-005 delivery with enhancements to support new system functions and added functionality.

3.4.1 HMI Window Enhancement

Several windows are in development for integration in the HMI subsystem to allow the operator an interface to system control and monitoring, including system and subsystem state/model control, radar event requests, subsystem capabilities, and DSP Subsystem output data rendering.

3.4.2 HMI Subsystem Hardware Enhancement

HMI Subsystem Hardware supporting DO-011 Base Task development includes:

- Apple Power Mac G5 Tower
  - Dual 2.7 GHz PowerPC G5 Processors
  - 2 GB DDR400 SDRAM
  - ATI Radeon 9650 256 MB AGP Graphics Card

3.5 Communication Libraries and Networking

As in previous CARP Builds, messaging services are provided to the system by CARP Communication Libraries running GDAIS Multipurpose Transportable Middleware (MTM) across COTS network connections. Final Build 4 network configuration specification is still in progress. Two major functional upgrades have been added in the first semi-annual period of the DO-011 effort: automated performance measurement and 10 GE Network Interface configurations.

3.5.1 Automated Performance Measurement

To accurately characterize the performance of the Build 4 system, messaging latency metric measurement has been added to the CARP Communication Libraries' send and receive functions to record the network and processing latency associated with data progressing through the system. The libraries keep these values for all messages and can report statistics to the applications for analysis. The resulting system characterization will be used to benchmark, optimize and possibly re-size system components.

3.5.2 10 GE Networking

Configuration of 10 GE Networking equipment, including setup and cabling of Force10 10GE switches, is underway in preparation for upcoming Build 4 subsystem integrations.

3.5.3 Networking Hardware Enhancement

System Networking Hardware supporting DO-011 Base Task development includes:

- Force10 Network Switch
  - E1200 Switch Chassis (P# CH-E1200-BN3)
  - 48 Port Copper 1GE Card
  - 24 Port Copper 1GE Card
  - 48 Port Fiber 1GE Card
  - 24 Port Fiber 1GE Card
  - Gigabit Ethernet SFP Optics Module SX (2)
  - 4 Port Fiber 10GE Card
  - 2 Port Fiber 10GE Card
  - E1200 Power Entry Module (PEM)
  - Force10 Switch OS
- Ixia 10 GE Card (P# LM10GE700F1

3.6 Open Interface Specification

A foremost design criterion of the CARP Build 4 system is an emphasis on the fundamental tenants of open architecture development, especially open business practices and open interface specifications. Open system specification documents are in development in the DO-011 Base Task to define system and subsystem interfaces, control schemes and message flows.

3.6.1 Enhanced Control Scheme Support

Support for multiple control schemes is being built into the CARP Build 4 system. The system in development for DO-011 will allow embedded control, where radar event information progresses through the subsystems of the Radar System as fields attached to data products, and also orthogonal control, were control messages are issued separately, in advance of radar event execution. Work on this effort is still in progress.

3.6.2 System synchronization

Specification of a system synchronization configuration is in progress in DO-011. The previously delivered timing setup is being revisited. It utilized a combination of Inter Range Instrumentation Group (IRIG)-B time synchronization and Network Time Protocol (NTP) to maintain Time-of-Day.

4 CONTINUING DEVELOPMENT PLANS

Work on the Base Task of Contract No. N00014-01-D-0225 / Delivery Order 011 is still in progress and will continue to follow the Statement of Work. Goals of the next semi annual period of the contract include continued development and finally integration of the Open Interface-compliant CARP Subsystems (DDM including DREX simulation test scaffolding, RC, DSP and HMI) into a radar system with support for the DAR program built in. The final plan is to develop and integrate an antenna subsystem with the goal of live radar system testing.

The vision for the evolution of this technology is integration of an antenna subsystem and receiver/exciter prototypes and capabilities for continued development and evaluation of existing digital beamforming, DSP, and associated controls and user interfaces (Figure 4: Future Digital Radar System, below).

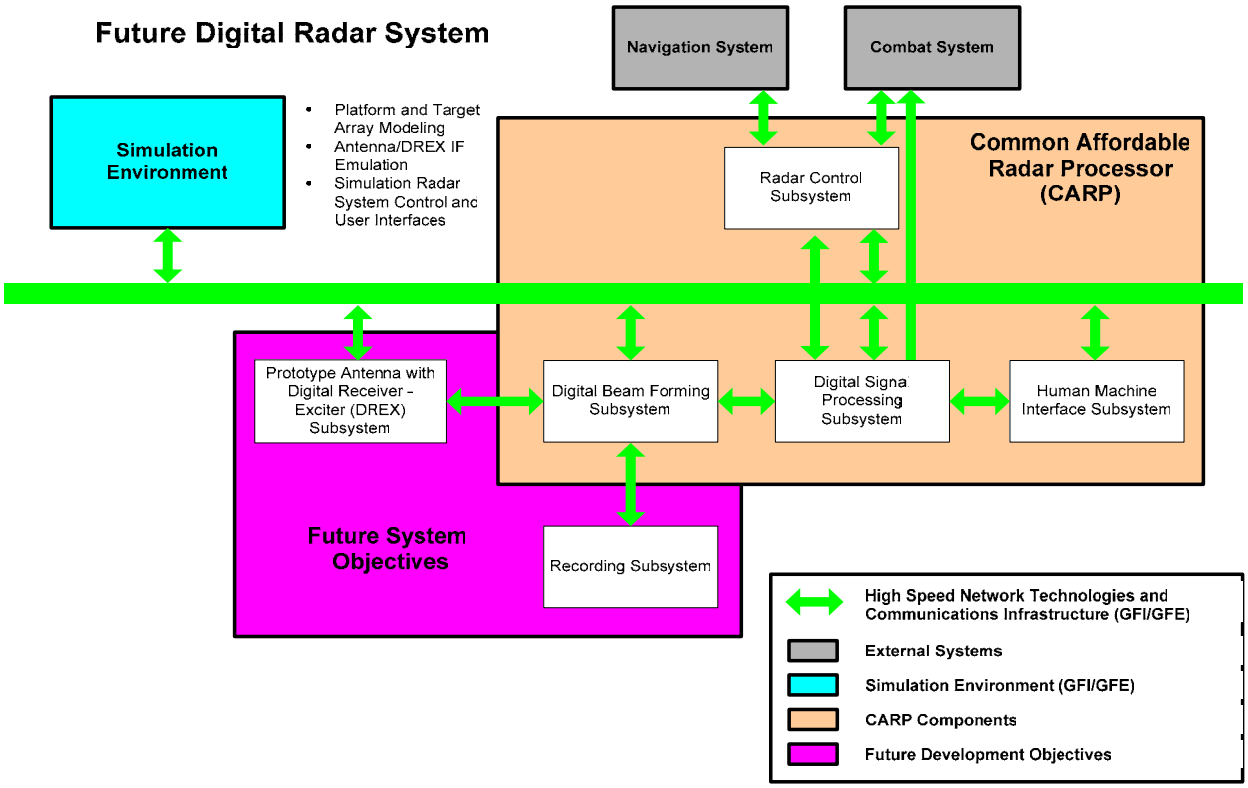

Figure 4: Future Digital Radar System

5 CONCLUSIONS

The CARP team has made significant progress towards completing program goals for DO-011 on schedule.

In the first semi-annual period of Contract No. 01-D-0225 / Delivery Order. 011, the team expanded the capabilities of the DDM Subsystem (including development of column beamforming and other performance and functional enhancements) and DREX test scaffolding, continued development of the DSP Subsystem (including process scheduling, benchmarking, and application performance and functional improvements) and Communication Libraries, worked to optimize the RC subsystem, expanded the HMI Subsystem, and continued open specification development and maturation.

6 ACRONYMS AND ABBREVIATIONS

API	Application Programming Interface
ATCA	Advanced Telecom Computing Architecture
CARP	Common Affordable Radar Processor
COTS	Commercial Off The Shelf
CVS	Concurrent Versions System
DDC	Digital Down Converter
DDM	Data Distribution Module
DDMC	DDM Controller
DO	Delivery Order
DP	Doppler Processor
DREX	Digital Receiver/Exciter
DSP	Digital Signal Processing
EQ	Equalization
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
HMI	Human Machine Interface
IF	Intermediate Frequency
IQ	Inphase/Quadrature
IRIG	Inter Range Instrumentation Group
ISE	Integrated Software Environment
MSPS	Mega Samples Per Second
MTM	Multipurpose Transportable Middleware
NIC	Network Interface Card
NTP	Network Time Protocol
ONR	Office of Naval Research
PC	Pulse Compressor
PEM	Power Entry Module
RC	Radar Controller
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
IP	Internet Protocol